ABSTRACT

Disclosed is a system and method for assembling a data packet. The system can be implemented as four memory elements associated with one or more processors. The first memory element stores a sequence number and a sub-channel identifier for an incoming data packet. The second memory element stores a revised packet fragment. The third memory element stores an unrevised packet fragment. The fourth memory element stores a starting address. In the system, the starting address may be the starting address of the revised packet fragment or the unrevised packet fragment wherein the first memory element identifies portions of the fourth memory element associated with the sequence number. The one or more processors are configured to create a modified data packet by combining the unrevised packet fragments and the revised packet fragment, wherein the modified data packet is associated with the sequence number and sub-channel identifier.